International Journal of Applied and Natural Sciences (IJANS)
ISSN(P): 2319-4014; ISSN(E): 2319-4022
Vol. 5, Issue 1, Dec – Jan 2016; 45-52

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

EXPERIMENTAL ANALYSIS OF EXCLUSIVE OR PHASE LOCKED LOOP (PLL)

W. IGONIYE[1], O. I. HORSFALL[2] & S. TAYLOR-HARRY[3]

[1]Department of Radiology, University of Port Harcourt Rivers State, Nigeria

[2]Departments of Physics, Rivers State University of Science and Technology, Port Harcourt, Nigeria

[3]Departments of Physics, Rivers State University of Education Rumuolumeni, Port Harcourt, Nigeria

ABSTRACT

An experimental analysis of phase locked loop (PLL) circuit has been carried out in order to build and test a simple PLL circuit, determine the lock and capture ranges for a PLL circuit with a traditional XOR phase/frequency comparator, lock and capture ranges for a PLL circuit with sampling type/ frequency comparator and to observe the phase relationship between the input and output waveforms for two common types of phase/frequency detectors. This will enable us ascertain the low power consumption, minimal frequency drift, excellent voltage-controlled oscillator(VCO) frequency linearity and zero voltage offset due to operational amplifier buffering.PLL consists of a phase detector, a loop filter and a voltage-controlled oscillator. The phase detector (PD) and loop combined produces an error signal which amplitude is linearly related to the phase difference of reference and VCO signals. The VCO adjust appropriate to synchronize both signals as desired. PLL in integrated chip 4046BE was studied and the working principles of PLL were verified. Parameters such as capture range and lock range were investigated. The capture range and the lock range of XOR-type PD and the sampling of PD was determined to range between 25 KHz to 40 KHz, 16 KHz to 61 KHz, 26KHz to 75KHz, and 30KHz to 79KHz respectively. The result of this study can be useful for synchronization purposes, provide immunity to substrate noise, power supply or ground voltage fluctuation and other desired effects, in space communication for coherent demodulation and threshold extension, demodulate frequency-modulated signals, synthesize new frequencies which are multiple of a reference frequency etc.

KEYWORDS: Phase Locked Loop, Phase Detector, Variable Controlled Oscillator, Lock Range, Capture Range

INTRODUCTION

Phase-Locked Loop (PLL) is a control system and one of the most commonly used circuit in both telecommunication and measurement engineering that generates an output signal whose phase is related to the phase of an input signal (Kolumban, 2005).

PLL is a closed-loop-feed-back-frequency electronic circuit consisting of variable frequency oscillator system and a phase detector (PD), Figure 1. The oscillator generates a periodic signal while the phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. (Kolumban, 1999)

PLL is a mixed signal circuitry with applications in the field such as frequency synthesis, FM demodulation, television sweep circuits, time-pulse shifting modulation, the internal time phase frequency modulation, the carrier wavesynchronization and time synchronization (Albert, 2006)

PLL can be classified on its method of operation into three types, analogue (APLL), Hybrid (HPLL), and digital (DPLL). Basically PLL consist of three states, free-running, capture range and phase lock. When a steady signal arrives at a steady rate but suddenly moves in time there is no way for the receiver to know what has been changed during the data transmission to cause the movement of signal, this movement can be caused by amplitude change, frequency change or phase change. But in engineering it is a common knowledge that the sudden change is caused by phase change and needed a phase locked loop to solve the phase jittering problem (Albert, 2006). A simple PLL circuit consists of three main components: phase detector, loop filter and voltage controlled oscillator (VCO). The phase detector produces a signal proportional to the difference in the phase between a reference signal and the output signal from the VCO. The signal from the phase detector is passed through a low pass filter and applied to the control input of the VCO. This feedback signal will change the frequency of the VCO output signal until it is equal to the reference signal applied to the phase detector. The frequency of the VCO output signal will then "track" the frequency of the signal applied to the reference input of the phase detector. If a counter is inserted between the output of the VCO and the input of the phase detector, the frequency of the VCO output signal will change until it is equal to the reference frequency the modulus of the counter. In this case the circuit acts as a frequency multiplier (Douglas, 1989).If a charge pump is connected between the phase detector and loop filter depending on whether the phase leads or lags, and up or down command is sent to the charge pump which supplies an analogue control voltage to the VCO to adjust the frequency of oscillator. PLL devices are available from many manufactures: Texas, Motorola, National, and Exar. Harris, Signetics. The upper operating frequency limit of currently possible devicesis of the order of 30 MHz (George, 1978)

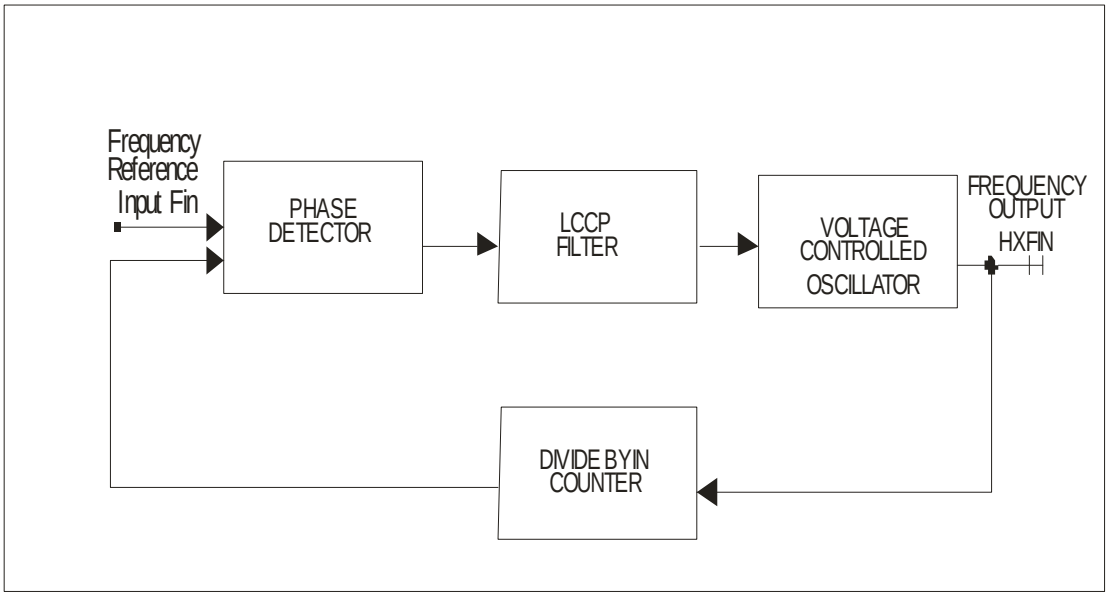

Figure 1: Block Diagram of PLL Frequency Multiplier (Tony Von Roon, 2001)

MATERIALS AND METHODS

The following materials were used to achieve the ultimate goal of this study:

- 1- 4.5V Power supply
- 1- TTL- Level signal generator
- 1- Oscilloscope

- 1- HC 4046BE
- 1- 3.3,5,10,22,51,75kΩ and 100Ω resistor each
- 2 - 2.2MΩ each
- 1- 2.2, 0.5, 2.02, and 0.001µF capacitors each
- 3 - 0.01µF capacitors.

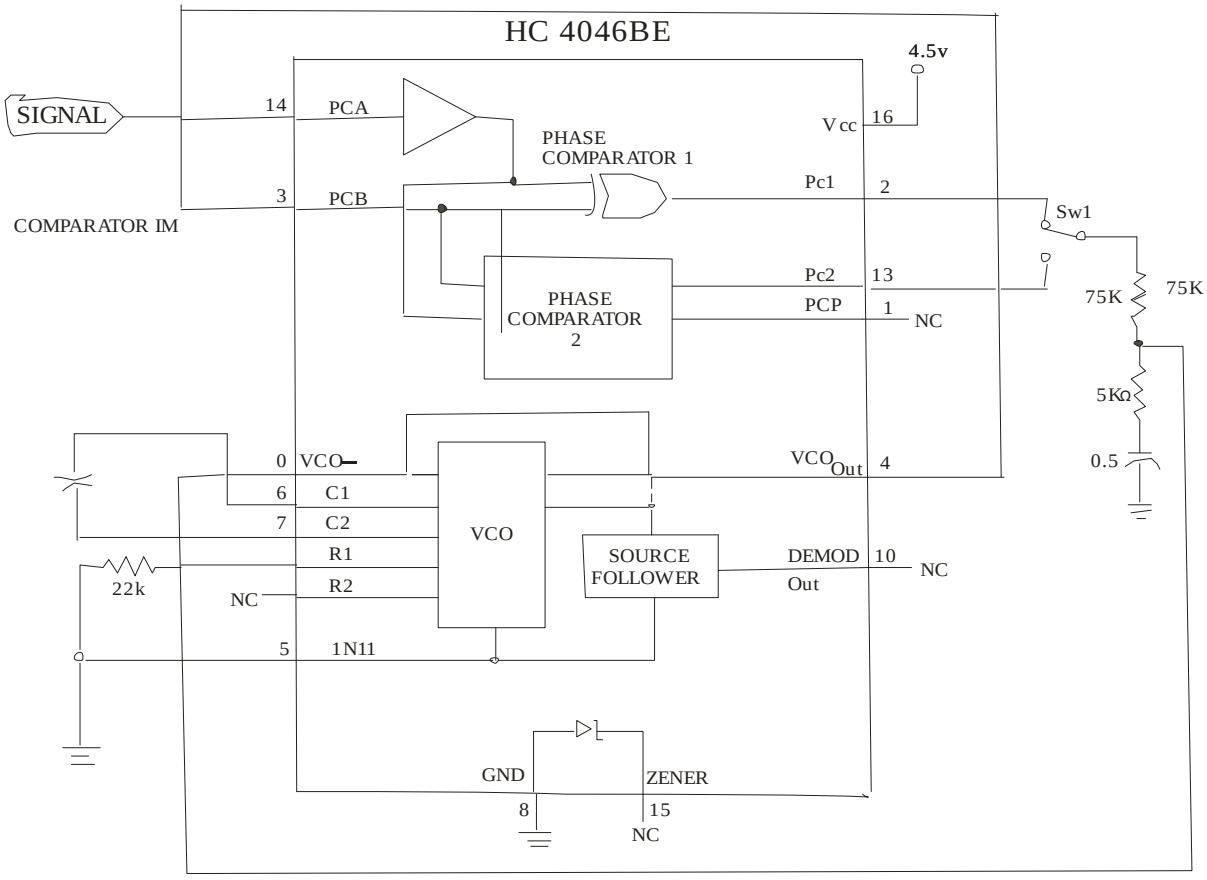

Figure 2: HC 4046BE No multiplying PLL Circuit (P.H. Young, 1994)

The Experimental/Circuit Analysis

The PLL in the circuit shown in Figure 2 above is entirely contained within one integrated(IC) chip. Signetics HC4046BC. The HC 4046BE is a phase locked loop circuit that comprises of linear voltage controlled oscillator (VCO) and two different phase detectors (PC1 and PC2) with a common signal input amplifier and a common comparator input.

The circuitry above showed the operation of the PLL in the following various steps.

- The output of Phase Comparator 1(PC1) is connected to Switch1 (SW1) on the input of the low-pass filter.
- Power was applied to the circuit and a 20-kHz TTL level signal was connected to the signal input, PCA, of the circuit.
- Dual-trace scope was used to observe the input signal and the VCO signal.

- Input frequency signal was increased to 60 kHz and the phase relationship between the input and output signals at this frequency were determined.
- Input frequency signal was increased until the output the output is no longer locked, the input frequency signal at which this occurred was recorded as upper locks frequency
- Input frequency signal was decreased until the circuit again locks on the input signal of the frequency where this occurred was recorded.
- Input frequency signal was decreased until the circuit lock input frequency where this occurred was recorded.
- Input frequency signal was slowly increased until the circuit again again locks on the input signal, this frequency was recorded as the lowercapture frequency.
- The capture range and the lock range for this circuit was determined.
- The signal generator was turn off and then the power to the circuit. The input of the low pass filter was switched from PC1 TO PC2.
- Steps 2 were repeated through steps 9.
- The lock and capture ranges for this circuit was compared with the lock and capture ranges of the previous circuit.

DETERMINATION OF OUTPUT FREQUENCY

The output frequency of the XOR phase detector and the sampling phase detector were measured with an oscilloscope by first determining the period as follows:

$$T = \left\{\left(\frac{time}{Division}\right) x \left(\frac{No\ of\ Division}{Cycle}\right)\right\} \quad (1)$$

Hence $frequncy = \frac{1}{T}$ (2)

The $\frac{time}{div}$ control was set to $\frac{2\mu s}{div.}$and input voltage for the experiment was 4.5 V

DETERMINATION OF OUTPUT VOLTAGE MEASUREMENT

The output voltage measurement of the XOR phase detector and the sampling phase detector were measured with and oscilloscope to determine the peak to peak amplitude of the signal as follows:

$$V_p - P = \left\{\left(\frac{Volts}{Divisions}\right) x \left(\frac{No\ of\ Divisions}{1}\right)\right\} \quad (3)$$

However, the vertical attenuation was set to $\frac{0.5V}{div}$

RESULTS AND DISCUSSIONS

The experimental data and its interpretation for this study is presented and discussed in the following tables below:

Table 1: XOR-Type Phase Detector

Input Frequency (kHz)	Output Frequency(kHz)	$\frac{No\ of\ Division}{Cycle}$	Output Voltage(V)
20.0	22.0	45.0	22.5
30.0	29.0	40.0	17.5
40.0	40.0	29.0	12.5
50.0	50.0	22.0	10.0
60.0	60.0	15.0	8.5

Table 2: Sampling Type Phase Detector

Input Frequency (kHz)	Output Frequency (kHz)	$\frac{No\ of\ Division}{Cycle}$	Output Voltage(V)
20.0	22.0	45.0	22.5
30.0	25.0	40.0	20.5
40.0	34.0	29.0	20.0
50.0	44.0	22.5	11.3
60.0	66.0	15.0	7.5

Table 3: Lock Frequency and Capture Frequency

Phase Detector	Lower Lock Frequency (kHz)	Upper Lock Frequency(kHz)	Lower Capture Frequency(kHz)	Upper Capture Frequency(kHz)
XOR	16	61	61	40
Sampling Type	30	79	26	75

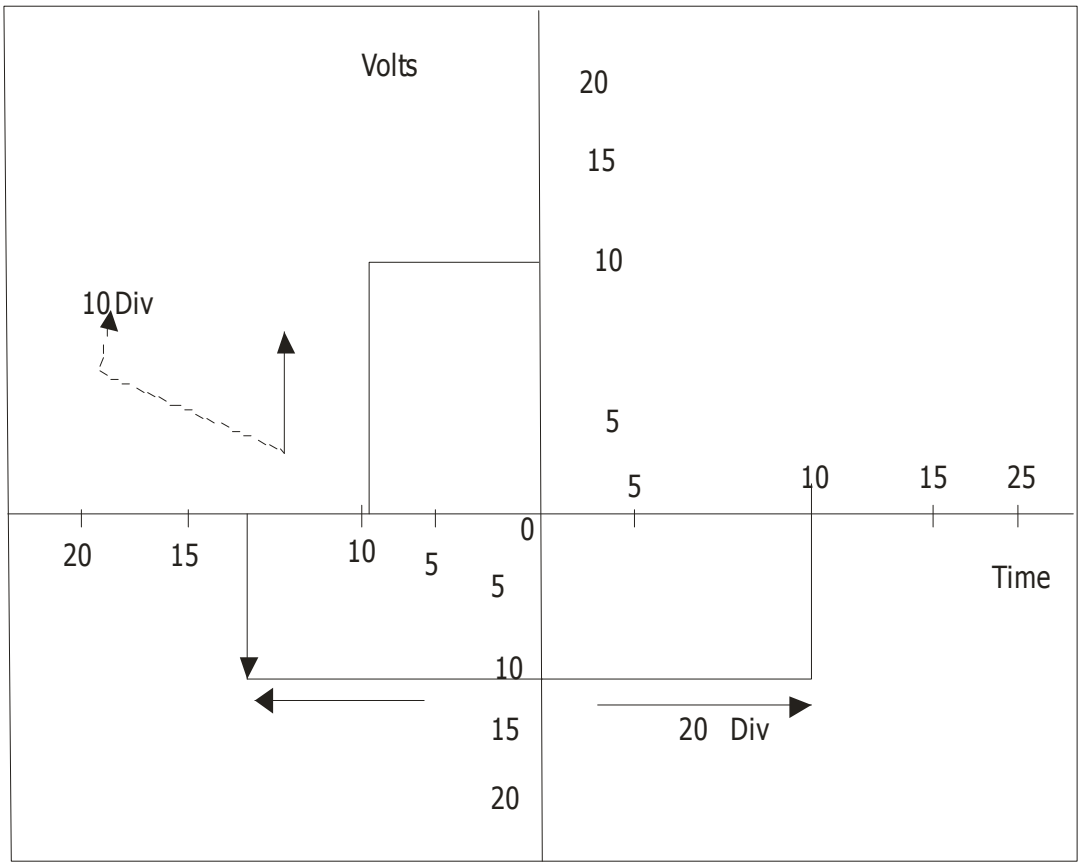

Figure 3: Output Voltage and Output Frequency Obtained from Oscilloscope

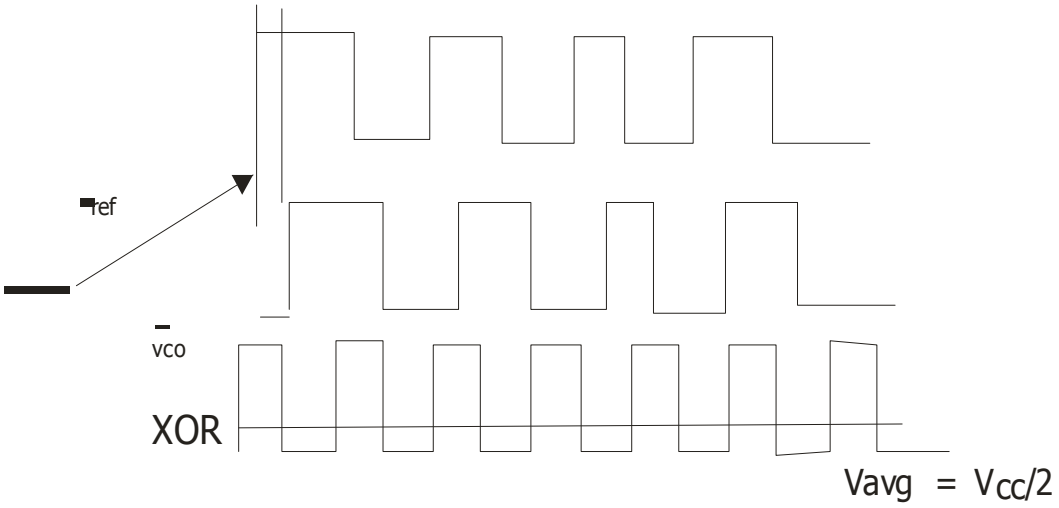

Figure 4: Phase Difference as Observed in XOR Phase Detector at 60 kHz

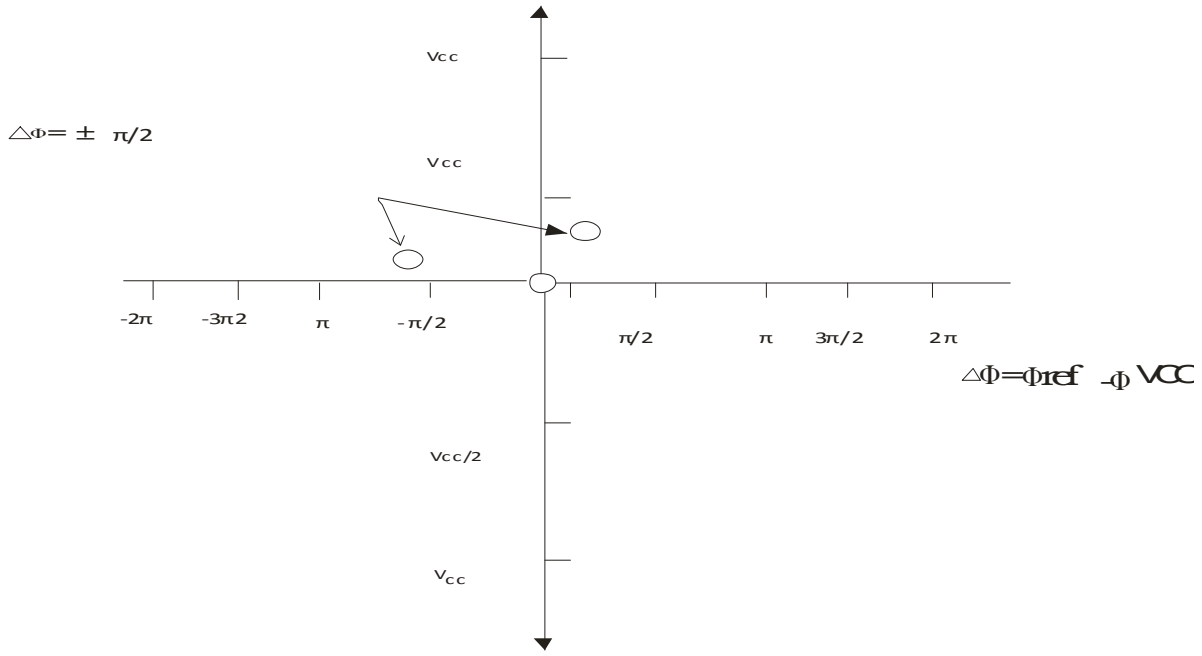

Figure 5: A plot of Average Output Voltage against Phase Difference

Table 1 showed measured output frequency and output voltage from Oscilloscope by varying the input frequency. The free running frequency was set at 7.5 kHz for XOR type phase detector and capture range was expected to fall close to it, and was found to be in the range of 25 kHz to 40 kHz as indicated in table 3. In figure 4 the free running frequency was set at 14 kHz for sampling type phase detector and capture range was expected to fall clos to it, and was found to be in the range of 26 kHz to 75 kHz as shown in table 3

The locked range of XOR and sampling type phase detector shows that XORgate PD can lock onto harmonics of reference signal and unlike the XOR type, the sampling PD is free from false locking to harmonics.

The lock range of the sampling type phase detector as shown in table 3 is 30 kHz to 79 kHz while that of XOR is 16 kHz to 61 KHz.

It can be observed that there is a linear relationship between the phase difference and the average output voltage at

input frequency of 60 kHz.

For the PLL to lock two conditions must be met: First, input and output frequency must be close enough to free running frequency to acquire lock. Even after acquiring the lock the PLL will only lock for a finite range called hold in or lock range. If the PLL was not in the lock condition then signals will not be synchronized.

From the analysis made on the results, it was observed that 16 pin package HC 4046 BE which contains, in addition to the VCO, two types of phase detector(type I and type II) which are level sensitive and edge sensitive respectively. With a source follower that made provision for measuring the VCO control voltage at pin 10 without loading anything. The average output from type I phase detector, fed to VCO input via the low-pass filter and seen at the phase differences of signals and the phase detector input. The average of V_{DEMout} is equal to $\frac{1}{2}V_{cc} = 2.25\ v$ in this experiment.

For phase Detector 1 (XOR), the phase range is π, thus the of $V_{DEMout} = \frac{V_{cc}}{\pi}$ switching from the type I phase detector to the type II phase detector (pin 13). The type II has leading edge sensing logic, which provides digital error signals PC2out and maintains a 0° phase shift between the input signals (PCA in and PCB in) independent of duty cycle.The phase detector gain is $\frac{V_{cc}}{4\pi}$

The XOR is more susceptible to locking onto harmonics of the phase difference of signals than the sampling type.

Figures 3, 4, and 5 shows the output voltage and input frequency obtained from the oscilloscope, the phase detector observed in the XOR phase detector at 60kHz and A plot of average output voltage against the phase difference respectively.

CONCLUSIONS

The following conclusions were drawn from the studies. The measured output voltage indicates low power consumption, when no input is applied to the phase detector the error voltage indicate zero what ascertain zero voltage offset due to the operational amplifier (opamp) buffering. A low level at the inhibit input enables the VCO and demodulator while a high level turns both off to minimize power consumption. The input and output characteristics of the VCO from the measured values shows an excellent VCO frequency linearity.

It was also observed that the capture and lock range of the sampling type detector is approximately equal while for the XOR type the lock range is greater than the capture range.

The XOR type phase detector is insensitive to frequency while the sampling type (phase frequency detector) greatly alleviates the phase locked problem. It is a special kind of arrival-time detector that generates dead-zone jittering glitch.

REFERENCES

1. Albert, 2006. Electronics manufacturers.comlito/circuirs and phase-locked-loops- PH, Htm. Retrieved 3/23/2007
2. Kolumban, G., “Phase –Locked Loops” Article in the Encyclopedia of RF and Microwave Engineering, K. Chand,(Ed.) Vol. 4, pp. 3735 – 3767, Wiley, New York, 2005
3. Douglas, V.H. (1989). Experimentas in Digital Circuit and systems. McGraw-Hill Publishing Company, New York. Pp. 68-71

4. George, B.C. (1980). Linear Integrated Circuit application, Macmillian Press Ltd, Liverpool Polytechnic pp.117
5. Kolumban, G., (1999) “Phase –Locked Loops” Article in the Encyclopedia of Electrical and Electronics Engineering, J.G. Webster,(Ed.) Vol. 16, pp. 158 – 188, Wiley, New York,
6. Young, P.H (1994) “Electronic Communication Techniques” 3rd Edition.
7. Tony Van Roon. (2001) VA3AVR. www.sentex.ca/mec1995/gadgets/pll/pll.html.